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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,450	03/19/2004	Paul J. Daniels	SC13292ZC	7280
23125	7590	04/27/2006	EXAMINER	
FREESCALE SEMICONDUCTOR, INC. LAW DEPARTMENT 7700 WEST PARMER LANE MD:TX32/PL02 AUSTIN, TX 78729			BEHM, HARRY RAYMOND	
		ART UNIT	PAPER NUMBER	
			2838	

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,450	DANIELS ET AL.	
Examiner	Art Unit		
Harry Behm	2838		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 10 April 2006.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 6 and 17 is/are allowed.

6) Claim(s) 1-5, 7-16 and 18-20 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 10 April 2006 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date .
4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: ____.

DETAILED ACTION

Drawings

1. The drawings were received on 4/10/06. These drawings are acceptable.

Specification

2. The specification was received on 4/10/06. The specification is acceptable.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3-5, 9-13, 15, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanzo (US 6,570,748) in view of Sanzo (US 6,570,748).
5. With respect to Claims 1, 11 and 13 Sanzo discloses an active circuit (Fig. 3 100') for being coupled to a reactive circuit (Fig. 3 14) that provides an output voltage (Fig. 3 LOAD Voltage), comprising: a control regulator circuit [implicit to a "switching circuit 14 [that] is a DC to DC buck converter that maintains a predefined voltage level across the load by switching current through an inductor"] having an output (connected to Fig. 3 16) for providing pulses [implicit to a switching DC

to DC converter]; a first switch (Fig. 3 S1) that has an input [gate] coupled to the output of the control regulator circuit, a power supply input (Fig. 3 Vin) coupled to a power supply terminal, and an output (Fig. 3 122) that is an output of the active circuit; a pulse shaper (Fig. 3 16) having an input [gate] coupled to the control regulator circuit and an output (Fig. 3 116); a reference voltage generator (Fig. 3 129) for providing a reference voltage (Fig. 3 Vref1) and an integrator (Fig. 3 108, 127) having a first input (Fig. 3 Vmonitor) coupled to the output (Fig. 3 122) of the pulse shaper, a second input for receiving the reference voltage (Fig. 3 Vref1), and an output (Fig. 3 Vstore) for providing a signal indicative of a current level supplied at the output voltage (Fig. 3 LOAD voltage). Sanzo does not disclose in the embodiment of Fig. 3 having Vref1 change in response to changes in a voltage at the power supply terminal. However, Sanzo does disclose in the embodiment of Fig. 4 where the Vref1 (paragraph 6 “threshold is dependent on the supply voltage”). IN Fig. 4, ISET is a threshold voltage corresponding to the maximum allowable current and is set proportional to the supply voltage. It would have been obvious to one of ordinary skill in the art at the time of the invention to make the voltage generator (Fig. 3 V1) change in response to changes at the supply voltage by making the reference voltage proportional to the supply voltage as taught in embodiment 4. The reason for doing so is

to make the “over-current technique [] immune to false triggering due to changes in line voltage” (paragraph 6).

6. With respect to Claim 3, Sanzo discloses the active circuit as set forth above, wherein the reference voltage generator (Fig. 3 V1,V2,168) is responsive to a first programming signal (Fig. 3 Vref2) in addition to being responsive to the voltage (Fig. 3 Vin) at the power supply terminal.
7. With respect to Claim 4, Sanzo discloses the active circuit as set forth above, wherein the reference voltage generator (Fig. 3 V1,V2,168) is responsive to a second programming signal (Fig. 3 Voffset).
8. With respect to Claim 5, Sanzo discloses the active circuit as set forth above, wherein the first programming signal (Fig. 3 128') is representative of the output voltage (Fig. 3 LOAD voltage).
9. With respect to Claim 9, Sanzo discloses the active circuit as set forth above, wherein the integrator comprises: a voltage-to-current converter (Fig. 3 127, 172,176) having a first input (Fig. 3 111) coupled to the output of the pulse shaper (Fig. 3 122), a second input (Fig. 3 Vref1) to the output of the reference voltage generator (Fig. 3 V1), and an output (Fig. 3 144); and a capacitor (Fig. 3 136) coupled to the output of the voltage-to-current converter.

10. With respect to Claim 10, Sanzo discloses the active circuit as set forth above, wherein the first switch (Fig. 3 16) comprises an N channel transistor (paragraph 4 “N-channel field effect transistor”).
11. With respect to Claim 12, Sanzo discloses the method as set forth above, wherein the integrating is performed by a capacitor (Fig. 3 136) from which current is removed (Fig. 3 176) and into which current is supplied (Fig. 3 172) during the integrating.
12. With respect to Claim 15, Sanzo discloses the active circuit as set forth above, wherein the information as to the DC output voltage (Fig. 3 LOAD voltage) is a first programming signal (Fig. 3 128').
13. With respect to Claim 16, Sanzo discloses the active circuit as set forth above, wherein the reference means (Fig. 3 129) is responsive to a second programming signal (Fig. 3 Voffset). Paragraph 8 “the offset voltage source 168 is used to adjust the voltage applied to the terminal ... one skilled in the art can see that other compensation techniques can also be used”.
14. With respect to Claim 19, Sanzo discloses the active circuit as set forth above, wherein the replication means comprises: a transistor (Fig. 3 16) coupled to the pulse means; and resistor means (paragraph 3 “Rds”) for being coupled between the transistor (Fig. 3 16) and the supply voltage (Fig. 3 Vin).

15. Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanzo in view of Morris (US 4,017,789).
16. With respect to Claim 2, Sanzo discloses the active circuit as set forth above. Sanzo does not disclose the use of a Schmitt trigger having an input coupled to the output of the integrator. “[Overcurrent protection circuits] for switching regulators usually employ a circuit such as a Schmitt-trigger” Morris paragraph 2. Morris teaches the use of a Schmitt-trigger which is used to detect variation in the output load. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a Schmitt-trigger at the output of the overcurrent integrator. The reason for doing so is to provide hysteresis which creates cleaner threshold transitions.
17. Claims 7, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanzo in view of Hosakawa (US 5,903,422).
18. With respect to Claims 7, 18 and 20 Sanzo discloses the active circuit as set forth above. Sanzo does not disclose a crowbar switch coupled to the control regulator circuit and a crowbar comparator coupled to the crowbar switch, nor does he disclose wherein the reference means comprises three current sources and a resistor. Hosakawa teaches that it is well known in the prior art to use a crowbar switch (Fig. 2 45) coupled to the control regulator circuit and a crowbar comparator (Fig. 2 43) coupled to the crowbar switch, and wherein the

reference means comprises three current sources (Fig. 1 24, 27 and 30) and a resistor (Fig. 1 28). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate a dedicated transistor, sense resistor and comparator to create for the purpose of detecting hard shorts and it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate another dedicated transistor for the purpose of sensing the current to detect a softer short.

19. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sanzo in view of Wang (US 6,670,794).
20. With respect to Claim 8, Sanzo discloses the active circuit as set forth above, wherein the pulse shaper comprises: a first transistor having a control electrode coupled to the output of the control regulator circuit, a first current electrode coupled to the output of the first switch, and a second current electrode. Sanzo does not disclose a first resistor having a first terminal coupled to the second current electrode of the first transistor and a second terminal coupled to the power supply terminal, but it is common to sense the resistance across the FET instead of using a sense resistor. Wang discloses it is possible to sense the current through the FET using a sense resistor (Fig. 2A) or using the resistance of the FET (Fig. 2B). It would have been obvious to one of ordinary skill in the art at the time of the invention to measure

the current flowing through the FET using a sense resistor instead of measuring the resistance of the FET, for the reason of having a simpler design where the resistance does not need to be measured only during the on time.

Response to Amendment

21. Applicant stated an inability to find in Sanzo where the reference voltage has a threshold dependent on the supply voltage. Sanzo discloses in the embodiment of Fig. 4 and paragraphs 14-15 where the reference voltage threshold depends on the supply voltage. In the prior office action, claims 1, 11 and 13 were rejected under 35 U.S.C. 102(b) using Sanzo embodiment Fig. 3. The rejection has been changed to 35 U.S.C 103(a) to combine the embodiment in Fig.3 with that in Fig. 4.

Allowable Subject Matter

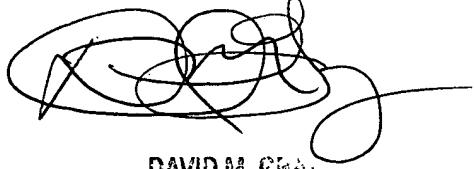
22. Claims 6 and 17 are allowed.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Behm whose telephone number is 571-272-8929. The examiner can normally be reached on Business EST.
24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Gray can be reached on 571-

2721989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



DAVID M. GHAI
PRIMARY EXAMINER